WHAT IS CLAIMED IS:

1. A timing generator for generating timing pulses for use to drive a solid-state imaging device, the generator characterized by comprising:

a first counter for performing a count operation responsive to each pulse of a vertical sync signal as a trigger;

a second counter for performing a count operation responsive to each pulse of a horizontal sync signal as a trigger;

a time-series data memory for storing time-series data that represents a logical level repetitive pattern of an output pulse train;

edge data storage for storing edge data that represents at what counts of the first and second counters control pulses should change their logical levels; and

means for changing the logical levels of the control pulses when the counts of the first and second counters match the edge data and for outputting, as the timing pulses, results of logical operations performed on the output pulse train, represented by the time-series data, and the control pulses.

2. The timing generator of Claim 1, characterized in that the time-series data memory has the function of

accepting the counts of the second counter as read addresses and supplying the output pulse train represented by the time-series data.

3. A timing generator system comprising: a timing generator for generating timing pulses for use to drive a solid-state imaging device; and an external memory provided externally for the timing generator, the system being characterized in that the timing generator includes:

a first counter for performing a count operation responsive to each pulse of a vertical sync signal as a trigger;

a second counter for performing a count operation responsive to each pulse of a horizontal sync signal as a trigger;

a time-series data memory for storing first time-series data that represents a logical level repetitive pattern of an output pulse train; and

edge data storage for storing first edge data that represents at what counts of the first and second counters control pulses should change their logical levels, and

that the external memory stores second time-series data as an alternative to the first time-series data and second edge data as an alternative to the first edge data, respectively, and

that the timing generator further includes:

means for selecting either the first or the second time-series data;

means for selecting either the first or the second edge data; and

means for changing the logical levels of the control pulses when the counts of the first and second counters match the edge data selected and for outputting, as the timing pulses, results of logical operations performed on the output pulse train, represented by the time-series data selected, and the control pulses.

4. The timing generator system of Claim 3, characterized in that the external memory is a ROM outputting serial data.

5. The timing generator system of Claim 3, characterized in that the timing generator further comprises storage means for storing the second time-series data and the second edge data that have been supplied from the external memory.

6. The timing generator system of Claim 3, characterized in that a signal is transmitted between the timing generator and the external memory only when the system is powered up or while no effective pixel signals are output from the solid-state imaging device.

7. A timing generator system comprising: a timing generator for generating timing pulses for use to drive a solid-state imaging device; and a controller connected to the timing generator, the system being characterized in that the timing generator includes:

a first counter for performing a count operation responsive to each pulse of a vertical sync signal as a trigger;

a second counter for performing a count operation responsive to each pulse of a horizontal sync signal as a trigger;

a time-series data memory for storing first time-series data that represents a logical level repetitive pattern of an output pulse train; and

edge data storage for storing first edge data that represents at what counts of the first and second counters control pulses should change their logical levels, and

that the controller generates second time-series data as an alternative to the first time-series data and second edge data as an alternative to the first edge data, respectively, and

that the timing generator further includes:

means for selecting either the first or the second time-series data;

means for selecting either the first or the second edge

data; and

means for changing the logical levels of the control pulses when the counts of the first and second counters match the edge data selected and for outputting, as the timing pulses, results of logical operations performed on the output pulse train, represented by the time-series data selected, and the control pulses.

8. The timing generator system of Claim 7, characterized in that the controller is a computer outputting serial data.

9. The timing generator system of Claim 7, characterized in that the timing generator further comprises storage means for storing the second time-series data and the second edge data that have been supplied from the controller.

10. The timing generator system of Claim 7, characterized in that a signal is transmitted between the timing generator and the controller only when the system is powered up or while no effective pixel signals are output from the solid-state imaging device.

11. The timing generator system of Claim 7, characterized in that the time-series data memory and the edge data storage in the timing generator are mask ROMs on

which data, verified at the timing generator by means of the controller, has been written, and

that the timing generator is operable while disconnected from the controller.